CLAIMS

What is claimed is:

1. A memory structure comprising:

a plurality of substrates stacked one on another;

a plurality of connectors connecting said substrates to one another; and

at least one memory chip package mounted on each of said substrates,

wherein said connectors have a size sufficient to form a gap between said substrates,

wherein said gap is larger than a height of said memory chip package.

2. The memory structure in claim 1, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

3. The memory structure in claim 1, wherein said memory chip package and said substrates include identical electrical connections.

4. The memory structure in claim 1, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

5. The memory structure in claim 1, wherein said connectors comprises solder balls.

6. The memory structure in claim 1, further comprising a thermal connection between a top of said memory chip package and a bottom of an adjacent substrate, such that said thermal connection fills said gap.

7. The memory structure in claim 1, wherein said memory chip package comprises a chip having an array of memory elements mounted within a package.

8. A memory structure comprising:

a plurality of substrates stacked one on another;

a plurality of connectors connecting said substrates to one another; and

at least one memory chip package mounted on each of said substrates,

wherein said connectors have a size sufficient to form a gap between said substrates,

wherein said gap is larger than a height of said memory chip package, and

wherein each memory chip package includes only a single memory chip.

9. The memory structure in claim 8, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

10. The memory structure in claim 8, wherein said memory chip package and said substrates include identical electrical connections.

11. The memory structure in claim 8, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

12. The memory structure in claim 8, wherein said connectors comprise solder balls.

13. The memory structure in claim 8, further comprising a thermal connection between a top of said memory chip package and a bottom of an adjacent substrate, such that said thermal connection fills said gap and said memory chip package includes a single memory chip.

14. The memory structure in claim 8, wherein said memory chip package comprises a chip having an array of memory elements mounted within a package.

15. A method of manufacturing a memory structure comprising:

forming a plurality of chip packages on a memory chip;

attaching at least one first memory chip package to a first substrate;

attaching a second substrate to said first substrate using connectors; and

attaching at least one second memory chip package to said second substrate,

wherein said connectors have a size sufficient to form a gap between said first substrate and said second substrate, wherein said gap is larger than a height of said first memory

chip package.

16. The method in claim 15, further comprising testing said first memory chip package and said second memory chip package before said attaching of said first memory chip package and said attaching of said second memory chip package.

17. The method in claim 15, wherein said first memory chip package and said second memory chip package and said first substrate and said second substrate include identical electrical connections.

18. The method in claim 15, wherein each of said first substrate and said second substrate has a plurality of said memory chip packages mounted thereon.

19. The method in claim 15, wherein said connectors comprise solder balls.

20. The method in claim 15, further comprising forming a thermal connection between a top of said first memory chip package and a bottom of said second substrate, such that said thermal connection fills said gap.